Le 2ème Séminaire International sur les Energies Nouvelles et Renouvelables
The 2nd International Seminar on New and Renewable Energies
Unité de Recherche Appliquée en Energies Renouvelables,
Ghardaïa – Algérie 15, 16 et 17 Octobre 2012

Modeling and Control of Three-Phase Multilevel Shunt Active Power Filter for Medium Voltage Applications

K. Benamrane, T. Abdelkrim, Aeh Benkhelifa, B. Bezza

Applied Research Unit on Renewable Energies
Industrial zone, B.P. 88, Ghardaïa, Algeria.
Kbenamrane47@yahoo.fr, tameur2@yahoo.fr

***Abstract*—This paper describes the applications of five-level diode clamped Active Power Filter (APF) to the enhancement of medium voltage network power quality by compensation of harmonic currents produced by a nonlinear load. In the first part, the authors present a topology of five-level diode clamped Voltage Source Inverter (VSI), and its triangulo-sinusoidal Pulse Width Modulation (PWM) control strategy. In the second part, to remedy to instability problem of the input DC voltages of this APF, the authors propose to use a clamping bridge filter. After that, the sliding mode regulator used to control the APF is developed. The simulation results confirm the suitable performance of the filter after balancing the DC bus and using the sliding mode regulator.**

***Keywords*—Active Power Filter, Clamping bridge filter, Multilevel converter, Pulse Width Modulation (PWM)**

I. INTRODUCTION

The intensive use of power converters and other non-linear loads in industry and by consumers in general, is causing an increasing deterioration of the power systems voltage and current waveforms.

The presence of harmonics in power lines results in greater power losses in distribution, interference problems in among other problems. The main consequence is the reduction of productivity in many industries, and therefore, the issue of power quality delivered to the end consumers is, more than ever, an object of great concern.

International standards concerning electrical power quality (IEEE-519, IEC 61000, EN 50160, among others) impose electrical equipments and facilities should not produce harmonic contents greater than specified values, and also specify distortion limits to the supply voltage. Meanwhile, it is mandatory to solve the harmonic problems cause by the equipments already installed.

One of the modern solutions for solving problems related to on the control theory and the inverter topology, these active filters are capable of compensating harmonic currents, power factor and unbalance, achieving balanced, sinusoidal currents at the source, with an unitary value of power factor [1][2].

In this paper, first part is dedicated to the presentation of the model of the three phases five-level diode clamped VSI with its PWM control method. In the second part, to remedy to instability problem of the input DC voltages of this APF, the authors propose to use a clamping bridge filter. This APF is applied for the enhancement of medium voltage network power quality by compensation of harmonic currents produced by a nonlinear load (Fig. 1). At the end the simulation results of sliding mode controlled APF are presented.

II. STRUCTURE OF FIVE-LEVEL INVERTER

Structure of five-level diode clamped inverter is shown in Fig.2. Each leg is composed of four upper and lower switches with anti-parallel diodes. Four series dc-link capacitors split the dc-bus voltage in half. The necessary conditions for the switching states for the five-level inverter are that the dc-link capacitors should not be shorted, and the output current should be continuous [3].

Each leg of the inverter has five possible switching states (Tab.1):

State P2: The upper switching devices S_{1x}, S_{2x}, S_{3x} and S_{4x} (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage V_{xn} = E/2.

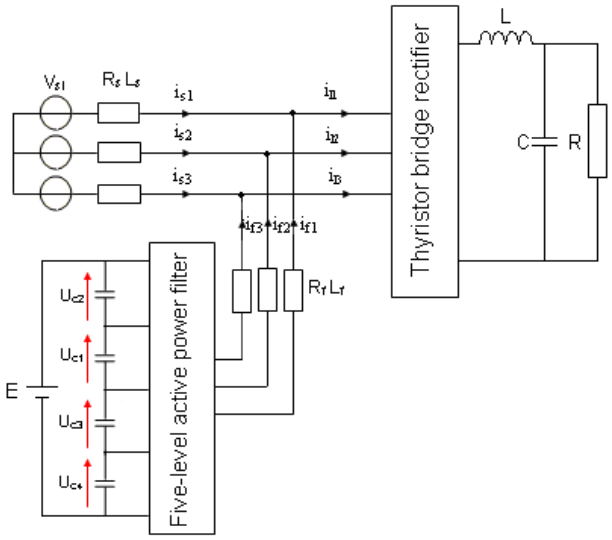

Fig. 1. Synoptic diagram of application of shunt APF

on power supply fed a nonlinear load

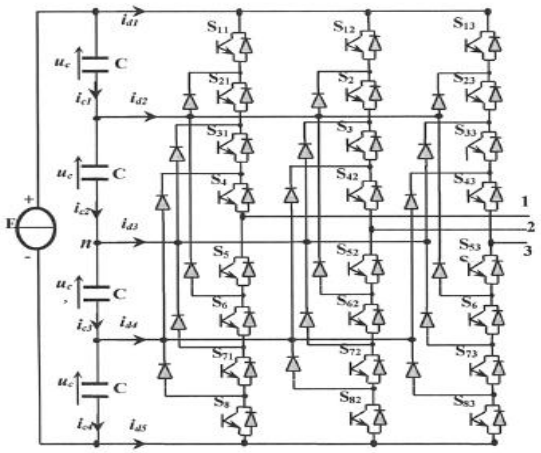

Fig. 2. Five-level diode clamped voltage source inverter

TABLE1
STATES OF FIVE-LEVEL INVERTER

Switching Symbols	Switching States								Output Voltage
	S_{i1}	S_{i2}	S_{i3}	S_{i4}	S_{i5}	S_{i6}	S_{i7}	S_{i8}	
P2	ON	ON	ON	ON	OFF	OFF	OFF	OFF	E/2
P1	OFF	ON	ON	ON	ON	OFF	OFF	OFF	E/4
O	ON	OFF	ON	ON	ON	ON	OFF	OFF	0
N1	OFF	OFF	OFF	ON	ON	ON	ON	OFF	-E/4
N2	OFF	OFF	OFF	OFF	ON	ON	ON	ON	-E/2

State P1: The switching devices S_{2x}, S_{3x}, S_{4x} and S_{5x} (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage V_{xn} = E/4.
State 0: The switching devices S_{3x}, S_{4x}, S_{5x} and S_{6x} (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage V_{xn} = 0.
State N1: The switching devices S_{4x}, S_{5x}, S_{6x} and S_{7x} (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage V_{xn} = -E/4.
State N2: The lower switching devices S_{5x}, S_{6x}, S_{7x} and S_{8x} (x = 1, 2 or 3) are turned on. The output phase to neutral point voltage V_{xn} = -E/2.

III. INVERTER OUTPUT VOLTAGES

For each switching device *Sij* (*i* = 1- 8, *j* = 1,2 *or* 3), we define a Boolean function *Fij* as:

$$F_{ij} = \begin{cases} 1 & \text{if } S_{ij} \text{ is ON} \\ 0 & \text{if } S_{ij} \text{ is OFF} \end{cases} \quad (1)$$

The complementarities between upper and lower switching devices of each leg impose the following equations:

$$F_{ij} = 1 - F_{(i-4)j} \quad i = 5 \text{ to } 8 \quad (2)$$

For each leg of the inverter, we define five connection functions (one for each switching state) as:

$$\begin{cases} F_{c1j} = F_{1j}F_{2j}F_{3j}F_{4j} \\ F_{c2j} = F_{2j}F_{3j}F_{4j}F_{5j} \\ F_{c3j} = F_{3j}F_{4j}F_{5j}F_{6j} \quad j = 1,2 \text{ or } 3 \\ F_{c4j} = F_{4j}F_{5j}F_{6j}F_{7j} \\ F_{c5j} = F_{5j}F_{6j}F_{7j}F_{8j} \end{cases} \quad (3)$$

The output phase voltages with reference to neutral point *(n)* of DC bus voltage are:

$$\begin{pmatrix} V_{1n} \\ V_{2n} \\ V_{3n} \end{pmatrix} = \begin{pmatrix} F_{c11} & F_{c21} & F_{c31} & F_{c41} & F_{c51} \\ F_{c12} & F_{c22} & F_{c32} & F_{c42} & F_{c52} \\ F_{c13} & F_{c23} & F_{c33} & F_{c43} & F_{c53} \end{pmatrix} \begin{pmatrix} E/2 \\ E/4 \\ 0 \\ -E/4 \\ -E/2 \end{pmatrix} \quad (4)$$

IV. PWM STRATEGY OF THE FIVE-LEVEL VSI

Two-level carrier-based PWM techniques to multilevel inverters by making the use of several triangular carrier signals and one reference signal par phase. For **N**-level inverter, **(N-1)** carriers with the same frequency $\mathbf{f_c}$ and same peak to peak amplitude $\mathbf{A_c}$ are disposed such that the bands they occupy are contiguous. The reference, or modulation, wave forme has peak to peak amplitude $\mathbf{A_m}$ and frequency $\mathbf{f_m}$, and its centered in the middle of the carrier set (Fig. 3). The reference is continuously compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device

corresponding to that carrier is switched on; and if the reference is less than a carrier signal, then the active corresponding to that carrier is switched off [4].

The different input DC voltages of the inverter are fed by a battery E (Fig. 2). Fig. 4 shows the simple output voltage V_A of the five-level VSI. Fig. 5 displays the voltages across input capacitors. It can be noted that these capacitors voltages are unbalanced.

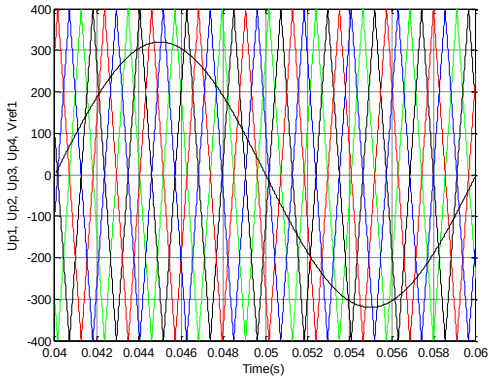

Fig 3. Triangulo-sinusoidal strategy with four bipolar carriers

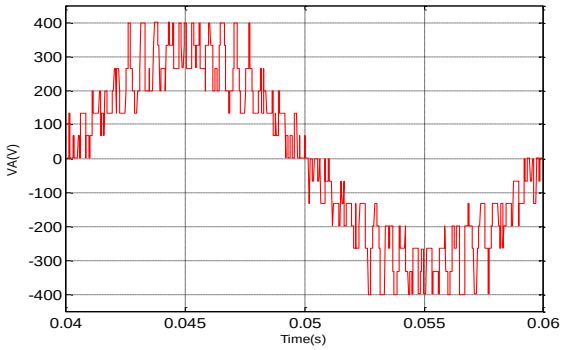

Fig 4. Simple output voltage VA

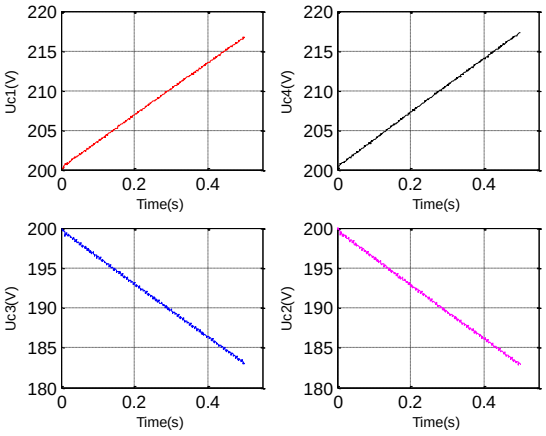

Fig 5. Inverter input capacitors voltages

V. MODELING AND CONTROL OF CLAMPING BRIDGE

The clamping bridge cell is a simple circuit constituted by a transistor and a resistor in series connected in parallel with a capacitor as shown in Fig. 6. The transistors are controlled in order to maintain the equality of the different voltages [5].

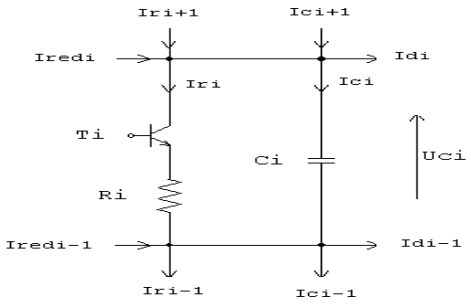

Fig. 6. Clamping bridge cell

In this part, the model of this filter with clamping bridge is defined by the following equation:

$$C_i(dU_{ci}/dt) = Ired_i + ir_{(i+1)} + ic_{(i+1)} - id_i - ir_i \quad (5)$$

with: $ir_i = T_i(U_{ci}/R_i)$

The transistor is controlled using the following algorithm:

$$\begin{cases} \varepsilon_i = U_{ci} - U_{cref} \\ \text{if } \varepsilon_i > dr \text{ on a } T_i = 1 \Rightarrow ir_i = T_i(U_{ci}/R_i) \\ \text{if } \varepsilon_i < -dr \text{ on a } T_i = 0 \Rightarrow ir_i = 0 \end{cases} \quad (6)$$

dr : hysteresis band width.

VI. ACTIVE POWER FILTER CONTROL

Active power filter is controlled using sliding mode regulator [6],[7]. From the model of active filter associated to supply network (7) and by considering the error between harmonic current reference and the active filter current as sliding surface (8), and the smooth continuous function as attractive control function (9), one gets the control law (10).

$$V_{frefK} - V_K = R_f i_{fK} + L_f(di_{fK}/dt) \quad (7)$$

with:

$V_K = V_{sK} - R_s i_{SK} - L_s(di_{sK}/dt)$; K = 1,2 and 3

$$S_s = i_{frefK} - i_{fK} \quad (8)$$

$$U_n = k.(S_s/(|S_s| + \lambda)) \quad (9)$$

$$V_{frefK} = R_f i_{fK} + L_f(di_{frefK}/dt) + V_K + k(S_s/(|S_s| + \lambda)) \quad (10)$$

VII. SIMULATION RESULTS

A medium voltage source of 5.5kV, 50Hz feeds a nonlinear load as illustrated in Fig. 1. This load produces a distorted current of 62 % THD which is above the tolerated THD limit standard. This current with its spectral analysis are presented in Fig. 7.

Fig. 8 shows DC bus capacitors voltages of APF before and after application of clamping bridges. Before t=0.1s, these voltages are unbalance. Application of clamping bridges allows getting stable capacitors voltages around there reference of 3kV.

Reference identified harmonic current i_{fref1} and output filter current i_{f1} are almost identical as presented in Fig. 9.

Fig. 10.a presents main source voltage V_{s1} and current i_{s1} after harmonic current compensation. Spectral analysis is presented in Fig. 10.b. It is shown that source current is almost sinusoidal with THD less than 4% and unity power factor.

Simulation Parameters:

Main source:

$V_{(ph-ph)}$ = 5.5kV, f = 50 Hz, R_s = 0.0001Ω, L_s = 0.001H.

Load:

L = 0.005H, R = 20 Ω, C = 0.01F .

Active power filter:

R_f = 0.0001 Ω, L_f = 0.004 H, C = 0.005 F, f_c =6 kHz.

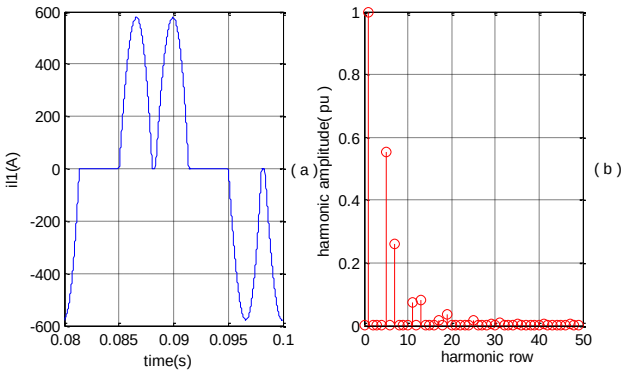

Fig. 7 Current drawn by the nonlinear load THD = 62%

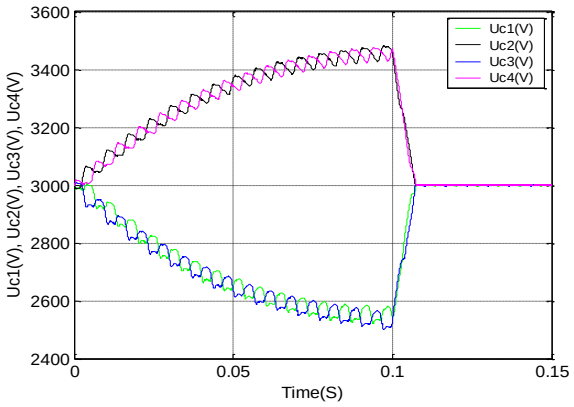

Fig. 8. DC bus capacitors voltages of five-level APF

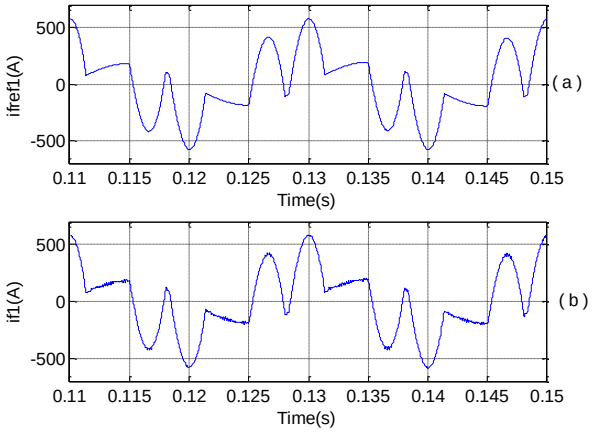

Fig. 9. Reference harmonic current ifref1 and

filter output current if1

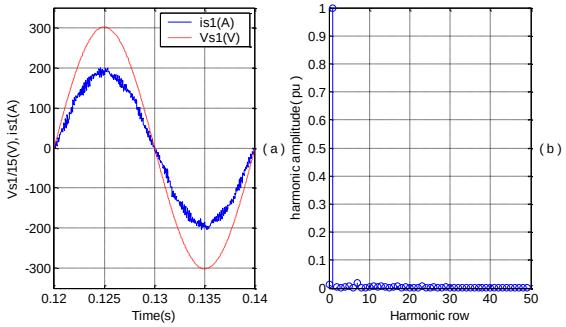

Fig. 10. Main source voltage Vs1and current is1 with

its spectral analysis (THD=3%)

VIII. CONCLUSION

We have proposed several methods to compensate the perturbations in an electrical network. In this paper a three-phase shunt active power filter that compensates line current harmonics has been presented and analyzed. Also the study of the instability problem of the input DC voltages of this converter shows that its different input voltages are not stables, which implies a bad harmonic current compensation. To solve this instability problem, one proposes to use a clamping bridge filter to improve input DC voltages balance.

Stable DC bus supply of sliding mode controlled five-level diode clamped shunt APF allows getting low-harmonic content network currents with THD less than 4% and unity power factor. The obtained results show that the proposed solution allows using this topology to compensate the harmonic current and reactive power in high power utilities.

REFERENCES

[1] H. Akagi, "Trends in Active Power Line Conditioners". IEEE Transactions on Power Electronics Vol. 9, No. 3, May. 1994, pp. 263-268.

[2] F. Z. Peng, "Applications Issues of Active Power Filters" IEEE Industry Applications Magazine, Sep/Oct 1998., pp. 21-30.

[3] D. Lalili, N. Lourci, E.M. Berkouk, F. Boudjema , J. Petzoldt, M.Yasin Dali, A Simplified Space Vector Pulse Width Modulation Algorithm For Five Level Diode Clamping Inverter, *International Symposium on Power Electronics, Electrical Drives, Automation and Motion*, 2006 pp. 21 – 26.

[4] N.Hur, J.Jung, K.Nam, "A Fast Dynamic DC-Link Power-Balance Scheme for a PWM Converter-Inverter System". IEEE Transactions on Industrial Electronics.Vol.N°.4, August 2001.

[5] F. Bouchafaa, E.M. Berkouk, M.S. Boucherit, Modelling and control of a power electronic cascade for the multi DC bus supply, *The International Journal for Computation and Mathematics in Electrical and Electronic Engineering, vol. 27 n 5*, 2008, pp. 1128 – 1143.

[6] J. J. Slotine, W. Li, *Applied Nonlinear Control* (Englewood Cliffs, NJ: Prentice-Hall, UK, 1991)

[7] V.I. Utkin, Sliding mode control design principles and application to electric drives, *IEEE Trans on Elect, vol. 40*, 1993, pp. 23 – 36.